Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A switched capacitor circuit capable of minimizing clock feedthrough effect comprising:

a first positive side switch element for selectively connecting a first positive side node to a third node depending upon a first control signal, wherein the first positive side node is connected to a positive side capacitor;

a second positive side switch element for selectively connecting the first positive side node to a second node depending upon a second control signal;

a third switch element for selectively connecting the third node to the second node depending upon a third control signal; and

a sequence controller connected to the switch elements for generating the first control signal, the second control signal, and the third control signal.

[c2] 2.The switched capacitor circuit of claim 1, wherein the first positive side switch element is larger than the second positive side switch element.

[c3] 3.The switched capacitor circuit of claim 1, wherein the

sequence controller switches off the switch elements sequentially in an order of decreasing size.

[c4] 4.The switched capacitor circuit of claim 1, wherein the second positive side switch element and the third switch element are substantially the same size.

[c5] 5.The switched capacitor circuit of claim 1, further comprising a means for making at least the smallest switch element gradually switch off.

[c6] 6.The switched capacitor circuit of claim 5, wherein each switch element comprises a transistor, and the means for making the smallest switch element gradually switch off comprises a low-pass filter connected to a control terminal of the smallest switch element.

[c7] 7.The switched capacitor circuit of claim 1, wherein the second node is ground and the switch elements comprise NMOS transistors.

[c8] 8.The switched capacitor circuit of claim 1, wherein the second node is a DC power supply node and the switch elements comprise PMOS transistors.

[c9] 9.The switched capacitor circuit of claim 1, further comprising:

a first negative side switch element for selectively con-

necting a first negative side node to the third node depending upon the first control signal, wherein the first negative side node is connected to a negative side capacitor; and

a second negative side switch element for selectively connecting the first negative side node to the second node depending upon the second control signal.

[c10] 10.The switched capacitor circuit of claim 9, wherein:

the first negative side switch element is substantially the same size as the first positive side switch element; and

the second negative side switch element is substantially the same size as the second positive side switch element.

[c11] 11.The switched capacitor circuit of claim 9, further comprising:

a center switch element for selectively connecting the first positive side node to the first negative side node depending upon a center control signal;

wherein the sequence controlleris further connected to the center switch element for generating the center control signal.

[c12] 12.The switched capacitor circuit of claim 11, wherein

the center switch element is larger than the first positive side switch element and the first negative side switch el-

ement.

[c13] 13.The switched capacitor circuit of claim 11, wherein the sequence controller first switches off the center switch element and then switches off the positive and negative side switch elements sequentially in an order of decreasing size.

[c14] 14.A method for minimizing clock feedthrough effect when switching off a switched capacitor circuit, the method comprising the following steps:
(a) disconnecting a first positive side node from a third node through a first positive side switch element;
(b) disconnecting the first positive side node from a second node through a second positive switch element; and
(c) disconnecting the third node from the second node through a third switch positive side element;
wherein the first positive side node is connected to a positive side capacitor.

[c15] 15.The method of claim 14, wherein the first positive side switch element is larger than the second positive side switch element.

[c16] 16.The method of claim 14, wherein the second positive side switch element and the third switch element are substantially the same size.

[c17] 17.The method of claim 14, wherein step (a) precedes steps (b) and (c).

[c18] 18.The method of claim 14, further comprising making at least the smallest switch element gradually switch off.

[c19] 19.The method of claim 18, wherein each switch element comprises a transistor, and making the smallest switch element gradually switch off comprises adding a low-pass filter to a control terminal of the smallest switch element.

[c20] 20.The method of claim 14, wherein the second node is ground and the switch elements comprise NMOS transistors.

[c21] 21.The method of claim 14, wherein the second node is a DC power supply node and the switch elements comprise PMOS transistors.

[c22] 22.The method of claim 14, further comprising the following steps:

(d) disconnecting a first negative side node from the third node through a first negative side switch element; and

(e) disconnecting the first negative side node from the second node through a second negative switch element;

wherein the first negative side node is connected to a negative side capacitor.

[c23] 23.The method of claim 22, wherein:
the first negative side switch element is substantially the same size as the first positive side switch element; and the second negative side switch element is substantially the same size as the second positive side switch element.

[c24] 24.The method of claim 22, wherein step (a) and step (d) are performed at the same time, and wherein step (b) and step (e) are performed at the same time.

[c25] 25.The method of claim 22, further comprising the following step:
(f) disconnecting the first positive side node from the first negative side node through a center switch element.

[c26] 26.The method of claim 25, wherein the center switch element is larger than the first positive side switch element and the first negative side switch element.

[c27] 27.The method of claim 25, wherein step (f) precedes step (a).